

EECS 142



Integrated Circuits for Communication

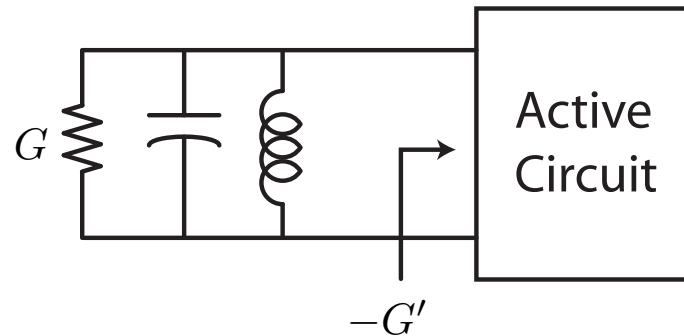
Lecture 23: Negative Resistance Osc, Differential Osc, and VCOs

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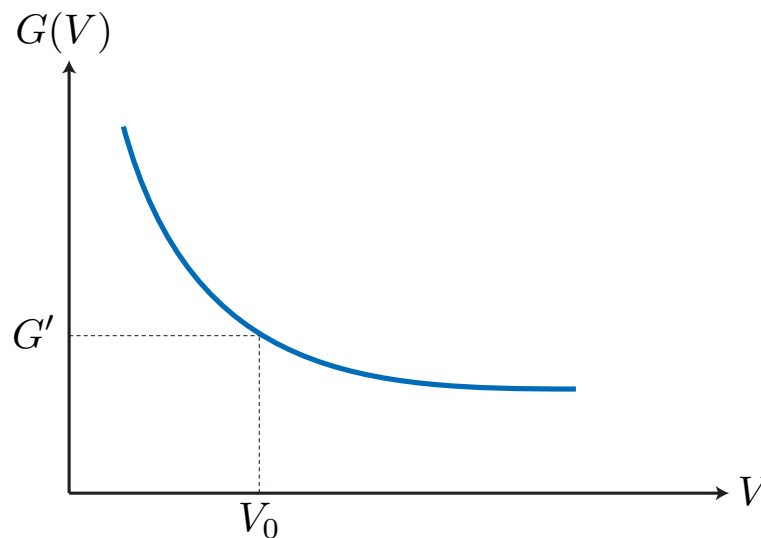
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Negative Resistance Perspective



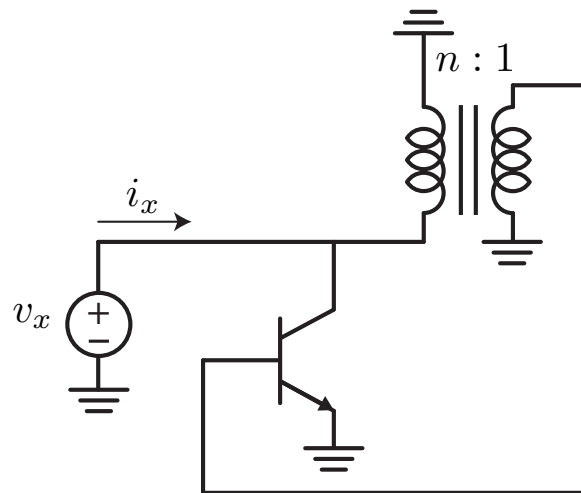
- In steady-state, the negative conductance generated by the active device G' should equal the loss conductance in the circuit, or $G' = G$
- If $G' = G(V)$ has the right form, then the oscillation amplitude V_0 will be a stable point.

Oscillator Stability (Intuition)



- Intuitively we can see that if the amplitude grows above V_0 by δV , then $G' < G$ and the circuit has net loss. The oscillation amplitude will thus decrease.
- Likewise, if the amplitude drops by some increment δV , then $G' > G$ and net energy is added to the circuit on each cycle. The oscillation amplitude will therefore grow.

Negative Resis LC Osc



- Consider a test voltage source connected to the transistor

$$i_x \approx i_c = g_m v_{in} = \frac{-g_m v_x}{n}$$

$$G_x = \frac{i_x}{v_x} = \frac{-g_m}{n}$$

Condition for Oscillation

- Now consider connecting the transistor with feedback to an LC tank with net loss conductance G_T . Oscillation will occur if

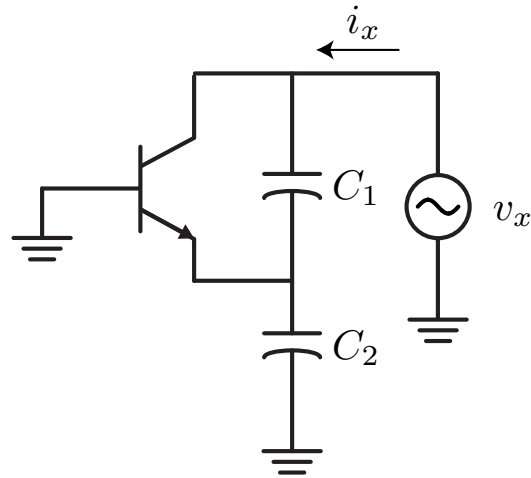
$$\frac{g_m}{n} > G_T = \frac{1}{R_T}$$

- But this is equivalent to

$$\frac{g_m R_T}{n} > 1$$

- Or the loop gain $A_\ell > 1$, a condition that agrees with our loop gain analysis.

Colpitts Osc



- Connect a test current source as before. Performing KCL

$$i_x = -g_m v_1 + (v_x - v_1)j\omega C_1$$

$$v_1 j\omega C'_2 + (v_1 - v_x)j\omega C_1 + v_1 g_\pi + g_m v_1 = 0$$

- Where $C'_2 = C_2 + C_\pi$. Notice that C_μ can be absorbed into the tank.

Colpitts (cont)

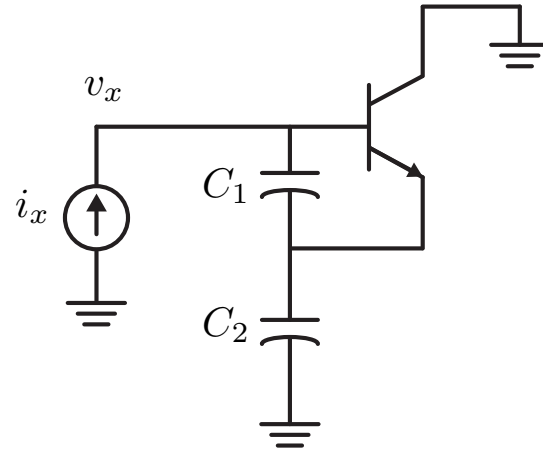
- Simplifying, we see that

$$\frac{v_1}{v_x} = \frac{j\omega C_1}{j\omega(C_1 + C'_2) + g_m + g_\pi} \approx \frac{C_1}{C_1 + C'_2} = \frac{1}{n}$$

- The above result follows directly from the capacitor divider. But notice that the assumption only holds when the capacitive susceptance dominates over the transistor transconductance.
- Using the above result we have

$$G_x = \frac{i_x}{v_x} = \frac{-g_m}{n} + j\omega \frac{C_1 C'_2}{C_1 + C'_2}$$

Clapp Oscillator



- Applying the same technique, note that

$$v_{\pi} \approx i_x Z_{C1}$$

$$v_x = v_{\pi} + (i_c + i_x) Z_{C2}$$

$$v_x = i_x (Z_{C1} + Z_{C2}) + g_m Z_{C1} Z_{C2} i_x$$

Clapp (cont)

- The input impedance seen by the source is given by

$$Z_x = \frac{v_x}{i_x} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} + \frac{g_m}{j\omega C_1 j\omega C_2}$$

- The negative resistance of the Clapp depends on frequency

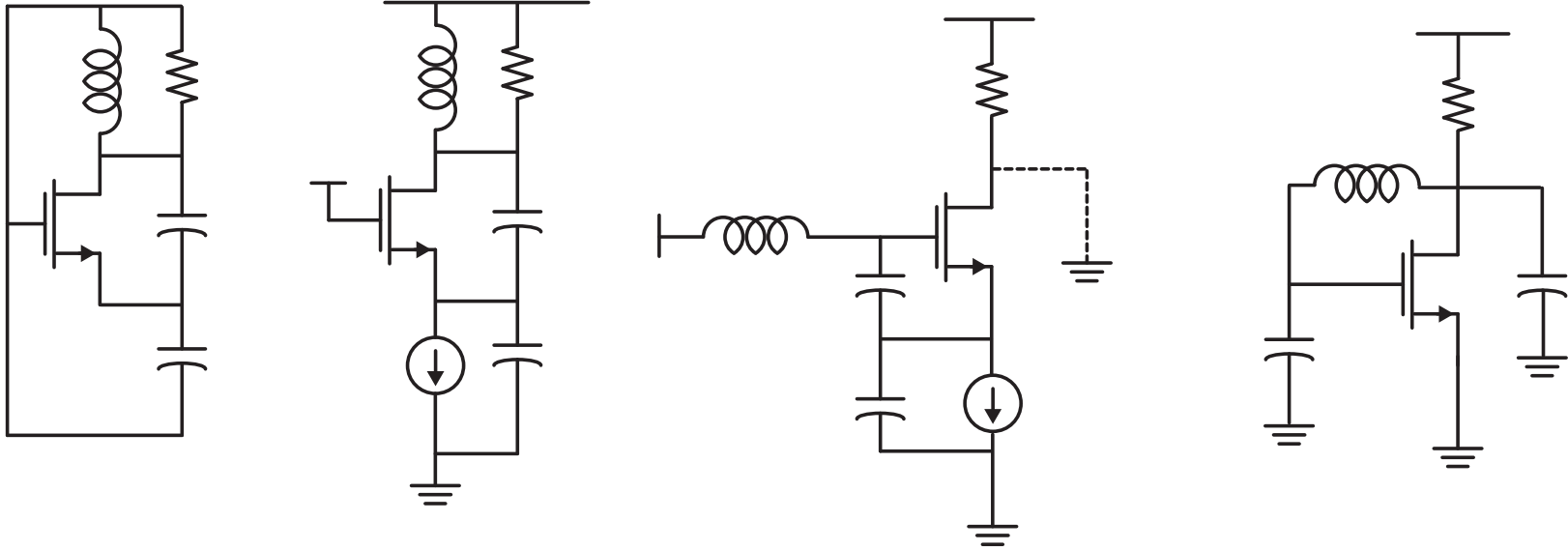
$$R_x = \Re(Z_x) = \frac{-g_m}{\omega^2 C_1 C_2}$$

- Oscillation will occur if the negative resistance generated by the transistor is larger than the series loss in the tank

$$|R_x| > R_s$$

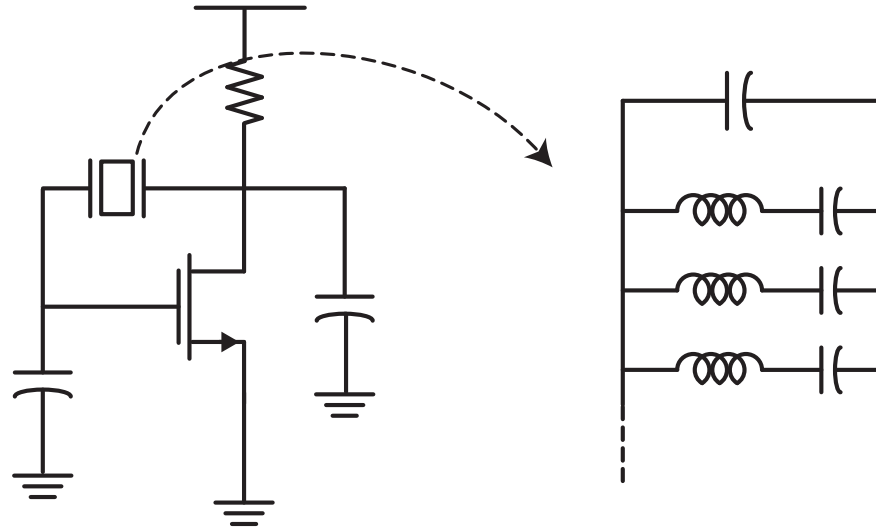
$$g_m > R_s \omega^2 C_1 C_2$$

MOS Oscillators



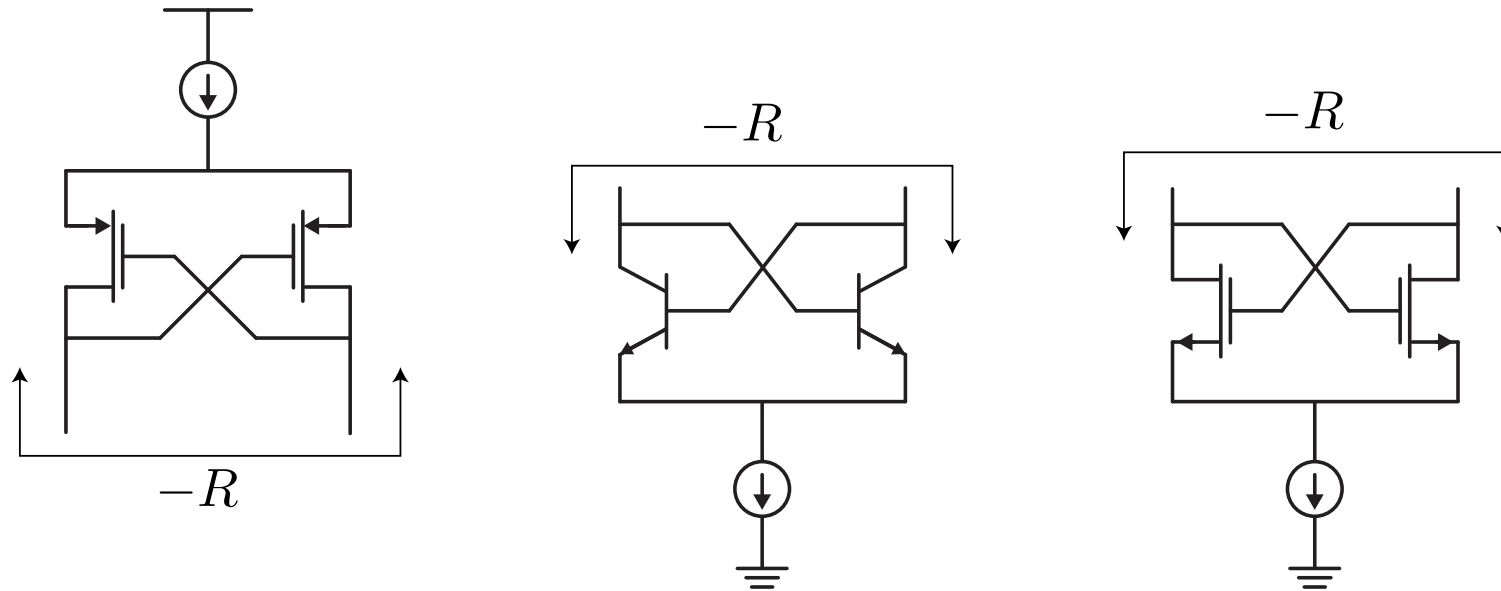
- Single transistor MOS oscillator topologies are identical to the BJT versions shown last lecture. The large-signal properties of the oscillator, though, differ significantly due to the different current limiting mechanisms in MOS transistors.

Crystal Oscillator



- The MOS Pierce oscillator is a popular crystal oscillator.
- The crystal behaves like an inductor in the frequency range above the series resonance of the fundamental tone (below the parallel resonance due to the parasitic capacitance).
- The crystal is a mechanical resonators. Other structures, such as poly MEMS combs, disks, or beams can also be used.

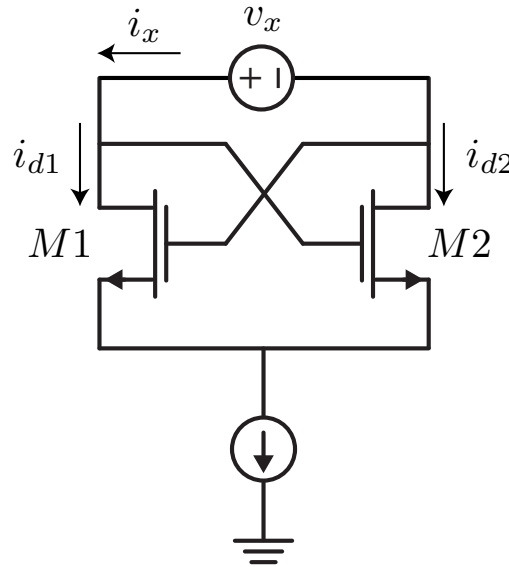
Differential Pair Negative R



- The MOS or BJT cross coupled pair generate a negative resistance. Since $i_x = i_{d2} = -i_{d1}$ and $v_x = v_{gs2} - v_{gs1}$

$$i_x = -G_m v_x = -\frac{g_m}{2} v_x$$

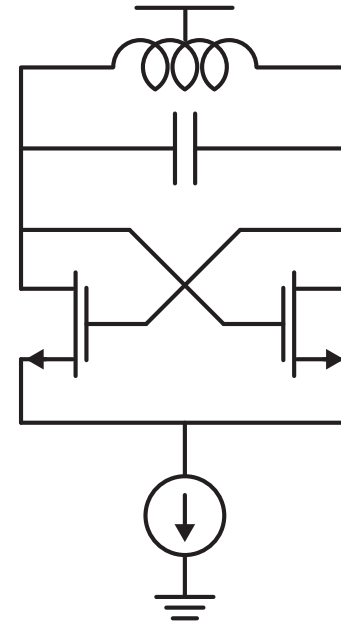
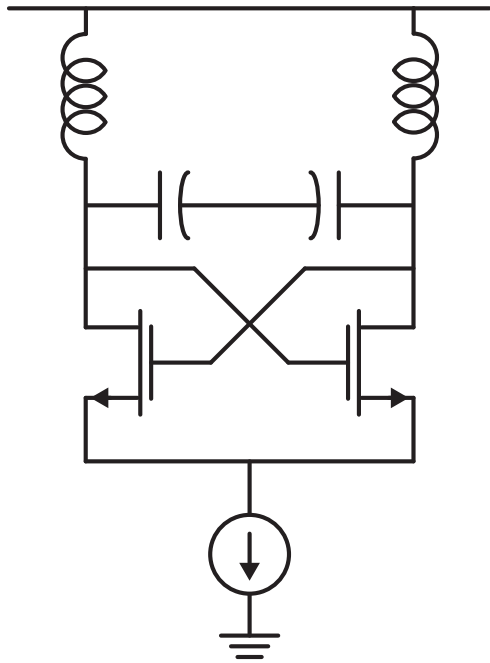
Cross-Coupled Resistance



$$G_x = \frac{i_x}{v_x} = -\frac{g_m}{2}$$

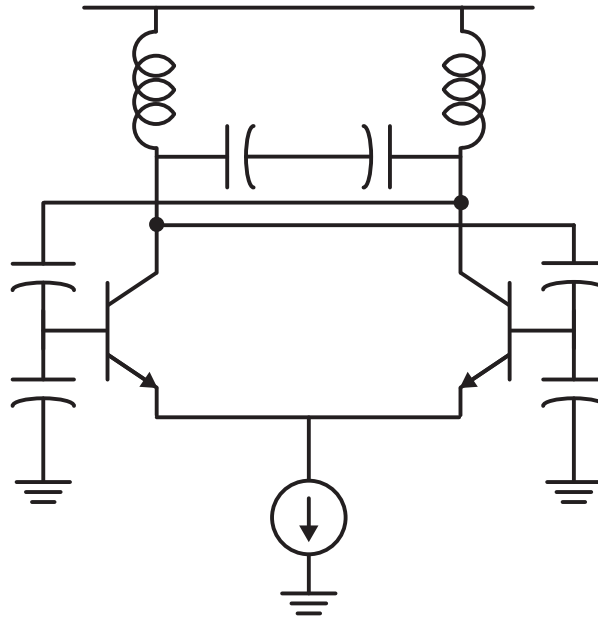
- The above equivalent circuit can be used to find the impedance of the cross-coupled pair.
- At high-frequency the device capacitance and input resistance should be included in the analysis.

Differential Oscillator



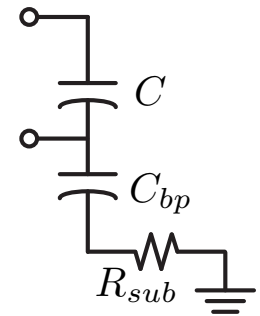
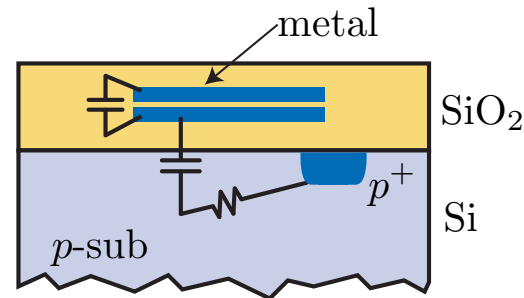
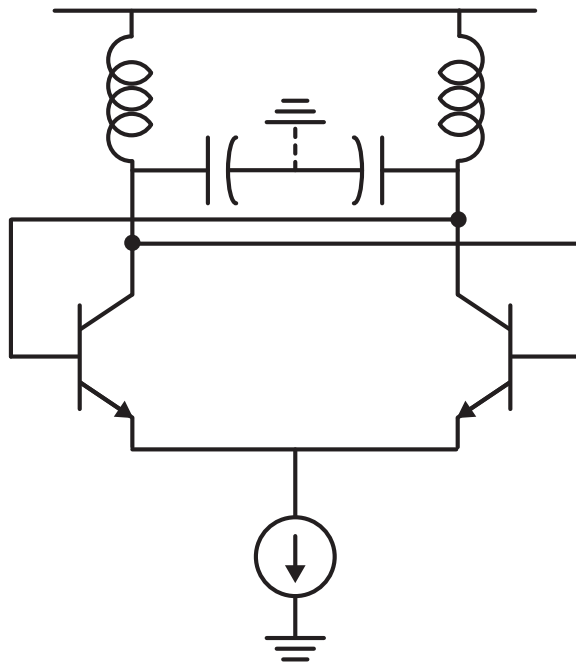
- We can connect two inductors or a single center-tapped inductor.
- A center-tapped inductor consumes less area than two separate inductors due to the mutual inductance between the windings.

BJT Differential Pair Osc



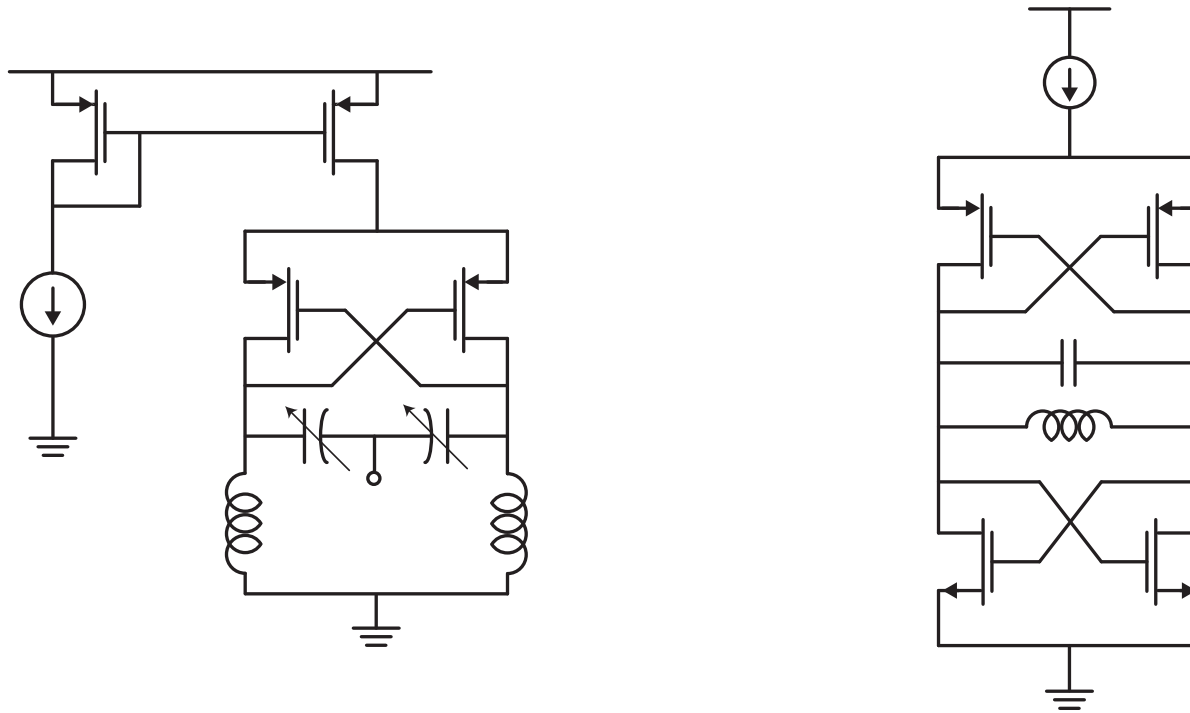
- A BJT version of the oscillator has limited voltage swing determined by the differential pair non-linearity. We can increase the voltage swing by emitter degeneration.
- A more popular alternative is to provide feedback capacitors. The negative conductance is decreased by the feedback factor.

Virtual Grounds



- We can take advantage of virtual grounds in differential circuits. For instance, the bottom plate parasitics of MIM capacitors should be connected to the virtual grounds to avoid tank de- Q -ing.

MOS Variations



- PMOS devices have less $1/f$ noise and so a PMOS current source will mix less power into the fundamental.
- Using both PMOS and NMOS differential pairs can lower the current consumption of the oscillator

$$G' = G_p + G_n$$

Voltage-Controlled Osc

- In most applications we need to tune the oscillator to a particular frequency electronically.
- A *voltage controlled oscillator* (VCO) has a separate “control” input where the frequency of oscillation is a function of the control signal V_c
- The tuning range of the VCO is given by the range in frequency normalized to the average frequency

$$TR = 2 \frac{f_{max} - f_{min}}{f_{max} + f_{min}}$$

- A typical VCO might have a tuning range of 20% – 30% to cover a band of frequencies (over process and temperature)

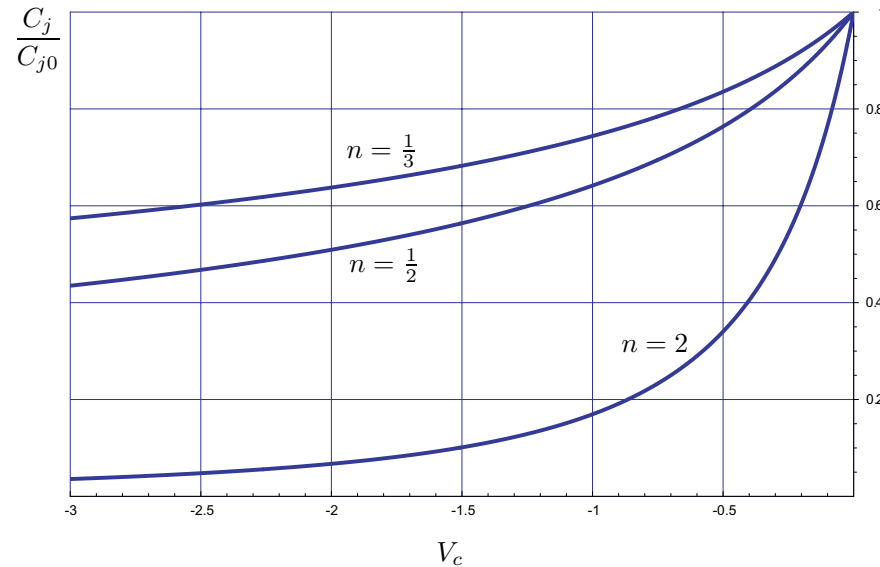
PN Junction Varactors

- The most common way to control the frequency is by using a reverse biased PN junction
- The small signal capacitance is given by

$$C_j = A_j \frac{\epsilon}{x_{dep}} = \frac{C_{j0}}{\left(1 - \frac{V_j}{\psi_0}\right)^n}$$

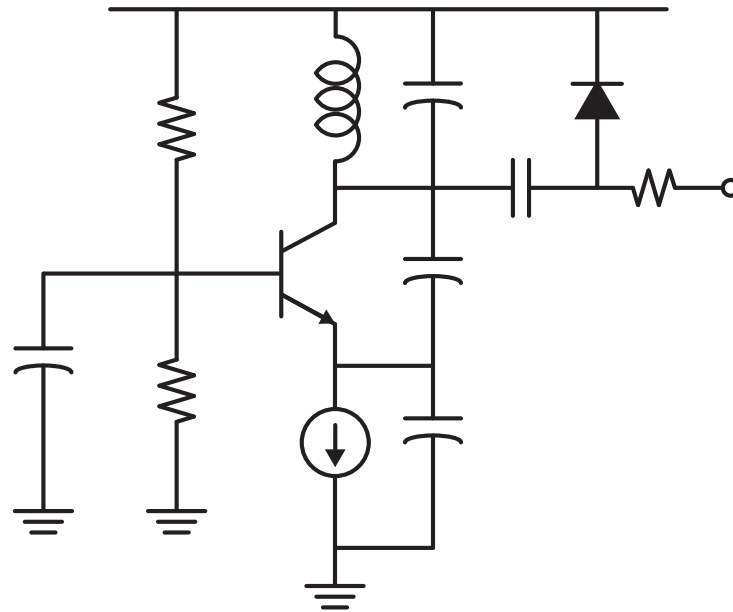
- The above formula is easily derived by observing that a positive increment in reverse bias voltage requires an increment of growth of the depletion region width. Since charge must flow to the edge of the depletion region, the structure acts like a parallel plate capacitors for small voltage perturbations.

PN Junctions Doping



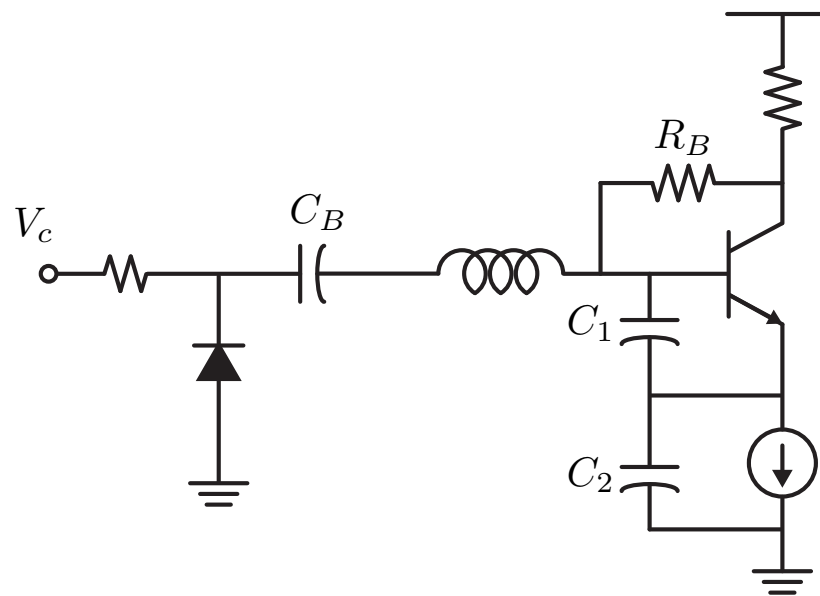
- Depending on the doping profile, one can design capacitors with $n = \frac{1}{2}$ (abrupt junction), $n = \frac{1}{3}$ (linear grade), and even $n = 2$.
- The $n = 2$ case is convenient as it leads to a linear relationship between the frequency of oscillation and the control voltage

Varactor Tuned LC Oscillator



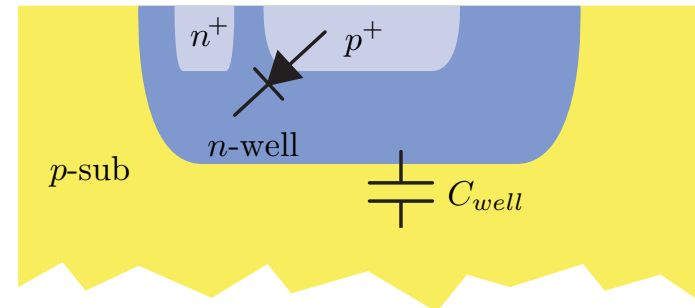
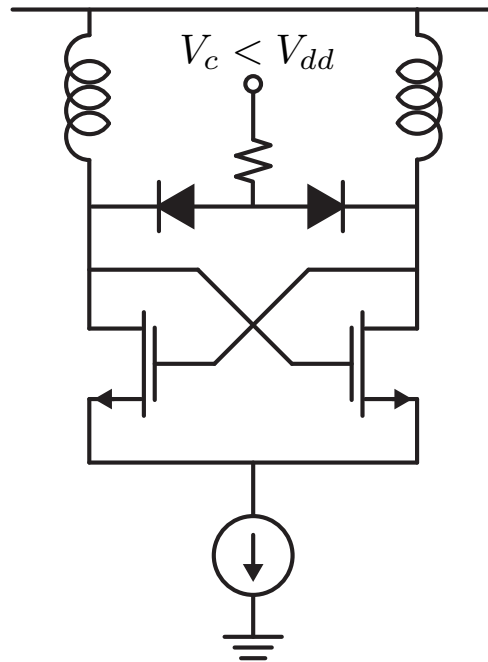
- The DC point of the varactor is isolated from the circuit with a capacitor. For a voltage $V < V_{CC}$, the capacitor is reverse biased (note the polarity of the varactor). If the varactor is flipped, then a voltage larger than V_{CC} is required to tune the circuit.

Clapp Varactor Tuned VCO



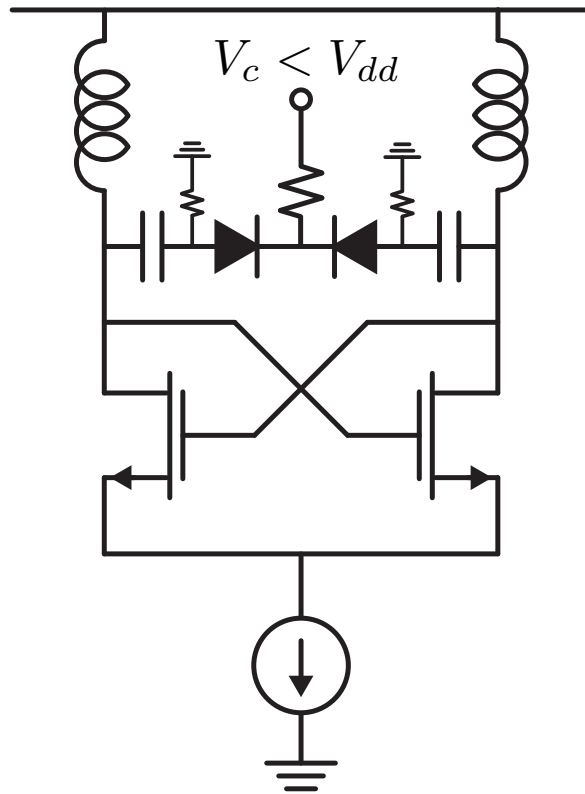
- Similar to the previous case the varactor is DC isolated
- In all varactor tuned VCOs, we must avoid forward biasing the varactor since it will de- Q the tank

Varactor Tuned Differential Osc



- Two varactors are used to tune the circuit. In many processes, though, the n side of the diode is “dirty” due to the large well capacitance and substrate connection resistance.

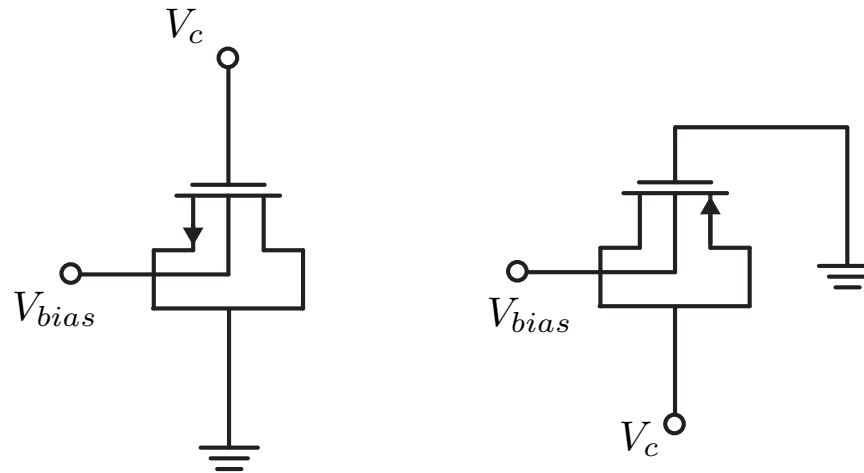
Varactor Tuned Diff Osc (cont)



- By reversing the diode connection, the “dirty” side of the PN junction is connected to a virtual ground. But this requires a control voltage $V_c > V_{dd}$. We can avoid this by using capacitors.

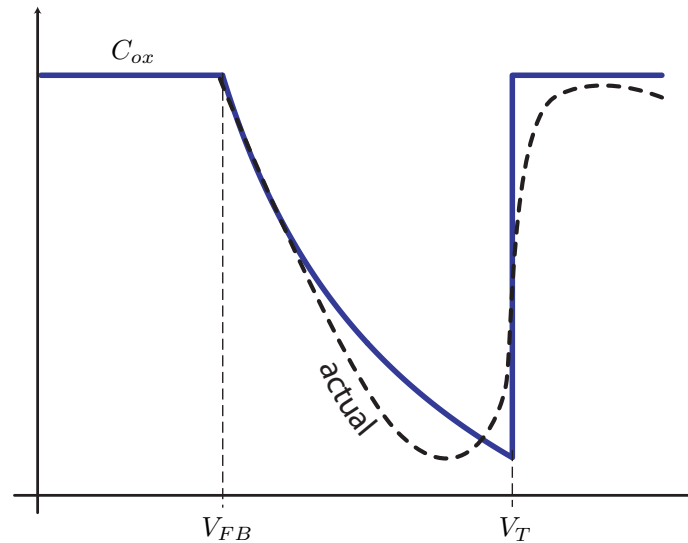
- The resistors to ground simply provide a DC connection to the varactor n terminals.

MOS Varactors



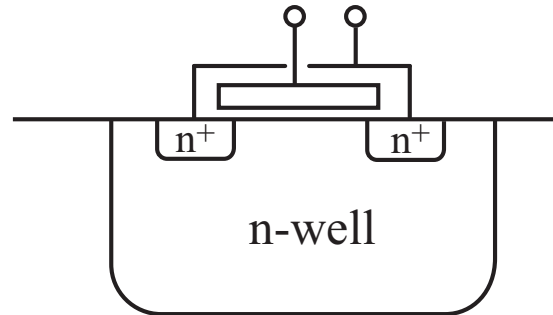
- The MOS capacitor can be used as a varactor. The capacitance varies dramatically from accumulation $V_{gb} < V_{fb}$ to depletion. In accumulation majority carriers (holes) form the bottom plate of a parallel plate capacitor.
- In depletion, the presence of a depletion region with dopant atoms creates a non-linear capacitor that can be modeled as two series capacitors (C_{dep} and C_{ox}), effectively increasing the plate thickness to $t_{ox} + t_{dep}$

MOS Varactor (Inversion)



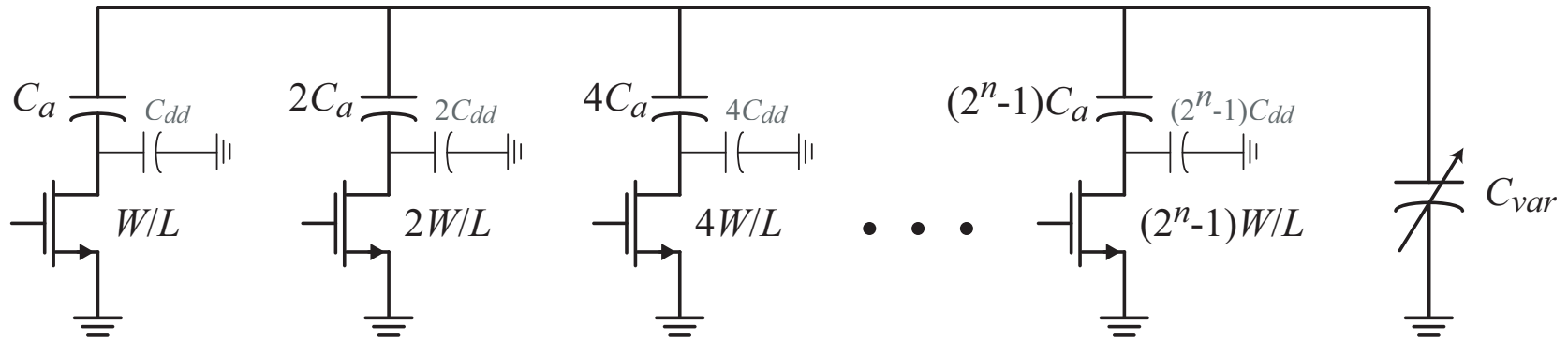
- For a quasi-static excitation, thermal generation leads to minority carrier generation. Thus the channel will invert for $V_{GB} > V_T$ and the capacitance will return to C_{ox} .
- The transition around threshold is very rapid. If a MOSFET MOS-C structure is used (with source/drain junctions), then minority carriers are injected from the junctions and the high-frequency capacitance includes the inversion transition.

Accumulation Mode MOS Varactors



- The best varactors are accumulation mode electron MOS-C structures. The electrons have higher mobility than holes leading to lower series resistance, and thus a larger Q factor.
- Notice that this structure cannot go into inversion at high frequency due to the limited thermal generation of minority carriers.

Switched Capacitor Varactor



- MOSFET switches can be used for discrete or coarse tuning of a VCO.
- The switch on-resistance should be minimized to maximize the Q of the capacitors. But too large of a switch means that the parasitic off-capacitance C_{dd} can be substantial, limiting the tuning range.
- There is an optimal switch size W to maximize the tuning range without incurring excessive loss.