Crystal Oscillator Design And Negative Resistance
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Timing is a critical part of almost every electronics application. Communication and data transfer generally require a reference signal or source to enable system synchronization and signal generation. At the heart of most reference sources is the oscillator, a circuit that produces an output signal with no input signal. Oscillator start-up is achieved by the injection of energy composed of noise and/or the transient power supply response. A crystal oscillator consists of a feedback network and an amplifier or gain element. Historically both of these building blocks were designed and manufactured by companies specializing in frequency control products but this paradigm has changed as separate companies design and manufacture the crystals and the amplifiers.

This TechNote focuses on the ubiquitous Pierce oscillator configuration, although the analysis can be applied to other oscillator configurations. The Pierce oscillator consists of an inverting amplifier and two capacitors all of which can be easily integrated with existing CMOS technology. The Barkhausen criterion is the most common design analysis tool or model that we have all become familiar with. Simply stated, the gain around the amplifying and feedback loop must be equal to or greater than one at the desired oscillation frequency. The phase shift through the loop must be zero or some integer multiple of 2π. An alternate and equally viable analysis methodology is the negative-resistance model. This model is attractive in that it can be easily simulated with common analysis tools like Spice. A current source is used as part of the ac simulation and one does not need to break the loop in analyzing start-up or small-signal negative resistance.

A negative-resistance measurement can be made in the lab using a Network Analyzer although the measurement methodology must be carefully examined. In the case of the Pierce oscillator a two-port measurement can be acquired with the gain and feedback network left intact. Negative resistance measured across frequency can give valuable insight into the behavior of desired and unwanted modes of oscillation. The widely-accepted series resistor method for calculating negative resistance is only valid at the frequency of operation. There is a discrepancy, however, in the measured negative resistance in comparison to the simulated start-up negative resistance. Differences in signal and impedance levels coupled with circuit nonlinearities are a major part of the measurement discrepancy. The measured negative resistance results using a network analyzer are lower than predicted by ac simulation; however, this will not be covered here. This TechNote will provide a theoretical explanation and design methodology for negative resistance. Traditionally, generic rules of thumb were applied to calculating the required amount of negative resistance in proportion to the resistance of the crystal. Negative resistance is critical in the design of VCXOs where the gain and resonator impedance will change across the input control voltage range.

The term negative resistance has been historically associated with an active device such as a vacuum tube, or a tunnel diode, whose characteristics change when operated in a

particular region of their I-V curve. These active devices exhibit a dip in the I-V curve such that an increase in voltage results in a decrease of current. This behavior, called negative resistance, is very useful in creating microwave oscillators (in the case of a tunnel diode). The important concept to remember when considering these types of devices is that no other passive components are required to create the effect of negative resistance. There are bias networks that are necessary to select the region of operation and associated feedback networks that create an oscillator network, but it is the active device itself that supplies the negative resistance. The I-V curve for a tunnel diode is illustrated in Fig. 1.
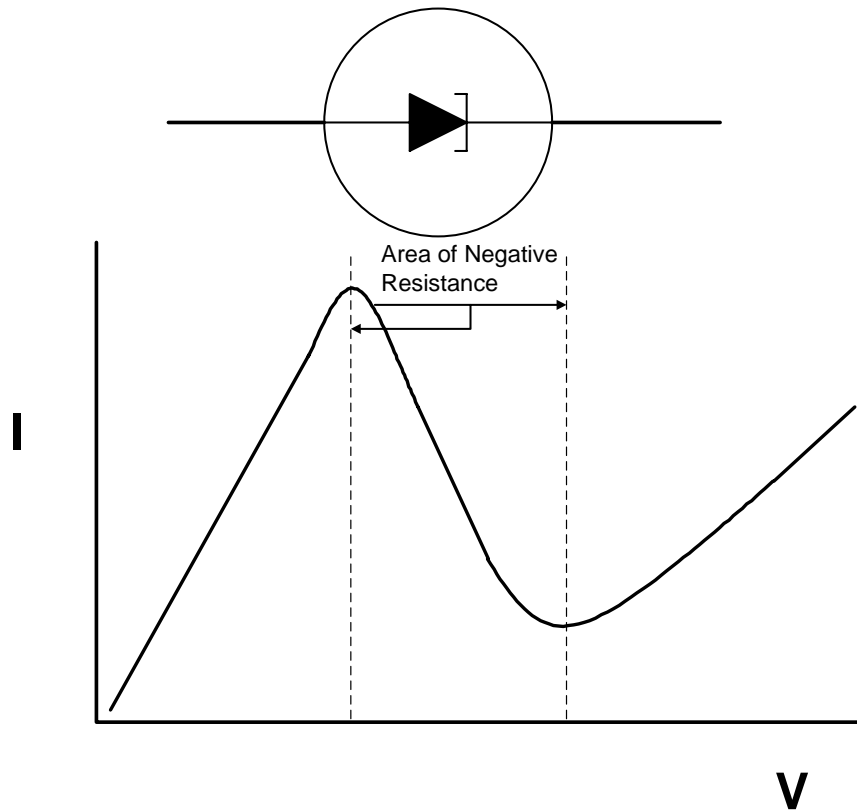
Tunnel Diode I vs V Curve

Fig. 1: Tunnel Diode I-V Curve

The term negative resistance has been used in the oscillator industry for many years to model the required gain needed from the active network to design stable oscillators. Historically the end user would purchase an oscillator from a vendor and the vendor then had complete control in the selection of the crystal and gain block and would subsequently design, test, and deliver the oscillator without the customer ever being involved in the crystal or gain element design or specification. Negative resistance has gained a lot of attention recently due to the fact that the end user is purchasing the gain block separately (now being integrated in silicon to offer greater functionality and flexibility) and then choosing a crystal from a different vendor.

This has created a new problem since the crystal vendor, semiconductor manufacturer, and the end user -- or customer -- determines the final design of the oscillator. They each may have different design guidelines and measurement methodologies. Negative resistance is a very important oscillator design parameter that can change based on the design guideline or measurement methodology employed. The end customer or isolated vendor may specify parameters that are not compatible for an overall successful oscillator design. The purpose here is to theoretically explain and quantify negative resistance when used in terms of oscillator design: such that the crystal vendor, semiconductor manufacturer, and customer can have a common platform for communication and collaboration in designing a robust crystal oscillator.

The first place to start is by defining a negative resistance model (see Fig. 2) for an oscillator and the basic requirements for oscillation to take place. [2]
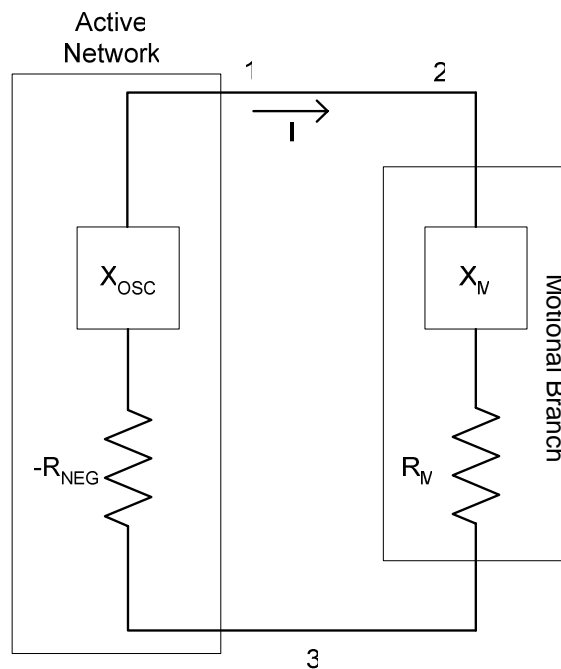

Fig. 2: Negative Resistance Model

The criteria for oscillation in the negative resistance model is analogous to that stated in the Barkhausen criterion. The condition at steady state is as follows:

$$-R_{NEG} = R_M$$
$$-X_{OSC} = X_M$$

The active network must produce a negative resistance that is equal -- in absolute value -- to the resistance of the motional branch. The reactive parts must cancel each other and it is at this point the frequency of operation is determined. When the signal amplitude is small, at start-up, the negative resistance is greater than the motional resistance and then decreases as the signal swing increases finally settling at the steady state value described above.

Herein lies the design constraint that causes the greatest confusion between vendors and customers alike. How much negative resistance should my active network provide to the motional branch at start-up? The motional branch that is commonly used is the quartz crystal. A quartz crystal provides a large Q tuned circuit that affords the end oscillator high-frequency stability. As stated previously, this was not a problem when there was only one designer and vendor involved in the oscillator design, but now you have the crystal vendor, semiconductor manufacturer, and the end customer all collaborating in the design. As with any design margin is built in to overcome design and process variations. In the case of specifying negative resistance this is also the case, but in addition the amount of negative resistance is chosen to overcome crystal drive level dependency and to optimize the oscillator start-up time.

The main problem arises when generic rules of thumb are applied to specifying negative resistance. These rules of thumb evolved empirically over the years and may not have their basis in fact. A plausible scenario is that a design specification was given to a vendor and confusion generated by jargon and measurement methodology caused a subsequent failure. The root cause of the failure was never identified and the end user merely increased their rule of thumb margin for negative resistance. A specification for five times the motional resistance was increased to ten times and then used as a blanket requirement when specifying active networks. At this point in the discussion the obvious question arises. What are the drawbacks to increasing the negative resistance? Gain is a good thing so is increasing gain even better? This article will demonstrate that, when used with a crystal, this is not the case and an increase in negative resistance can have catastrophic consequences to the end oscillator design. Specific equations will be given for the maximum negative resistance that any active network will provide when connected to a quartz crystal to form a crystal oscillator.

We have described the motional branch in our circuit as a quartz crystal. Fig. 3 is the electrical equivalent model of a fundamental mode quartz crystal.
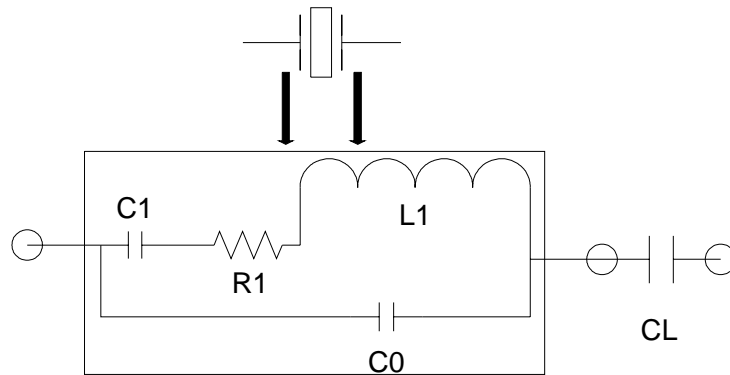
Fig. 3: Equivalent Crystal Network

C0: Static capacitance This is the capacitance of the metal electrodes, the dielectric constant of the quartz, and the holder and is not related to the piezoelectric properties of the quartz and can be measured by a C-I meter. It is sometimes referred to as the shunt capacitance and is typically measured in pF.

C1: Motional capacitance The capacitance that the resonator exhibits at the series resonant frequency. This is a direct result of the piezoelectric properties of the quartz and is represented in the traditional lumped equivalent circuit and sometimes referred to as Cm. This is dependant on the size of the crystal electrode and is typically measured in fF.

L1: Motional inductance The inductance that the resonator exhibits at the series resonant frequency. This is a direct result of the piezoelectric properties of the quartz and is represented in the traditional lumped equivalent circuit and sometimes referred to as Lm. This is transparent to the end user and taken into account when the crystal frequency and load are specified.

R1: Series resonant frequency resistance The resistance that the resonator exhibits at series resonant frequency. This is a direct result of the piezoelectric properties of the quartz and is represented in the traditional lumped equivalent circuit and sometimes referred to as Rs or ESR (Equivalent Series Resistance).

CL - Load capacitance for a specified parallel load resonant frequency This is useful in determining the exact load required to make the crystal operate at the specified frequency. Example: a 13.5 MHz crystal is ordered into a 14-pF load but due to the frequency calibration tolerance 13.500000 MHz occurs with 13.76 pF. The crystal manufacturer specifies this in ppm frequency tolerance at 25°C.

The active branch that is typically employed is the three terminal transistor connected in a Pierce oscillator configuration. The important point to stress here is that unlike the tunnel diode the following active network is comprised of an active device and a passive network. This is necessary in creating a condition of negative resistance. This analysis is valid for the Pierce gate oscillator as well.

The following diagram and set of equations listed in Fig. 4 will be presented to help describe the term negative resistance.
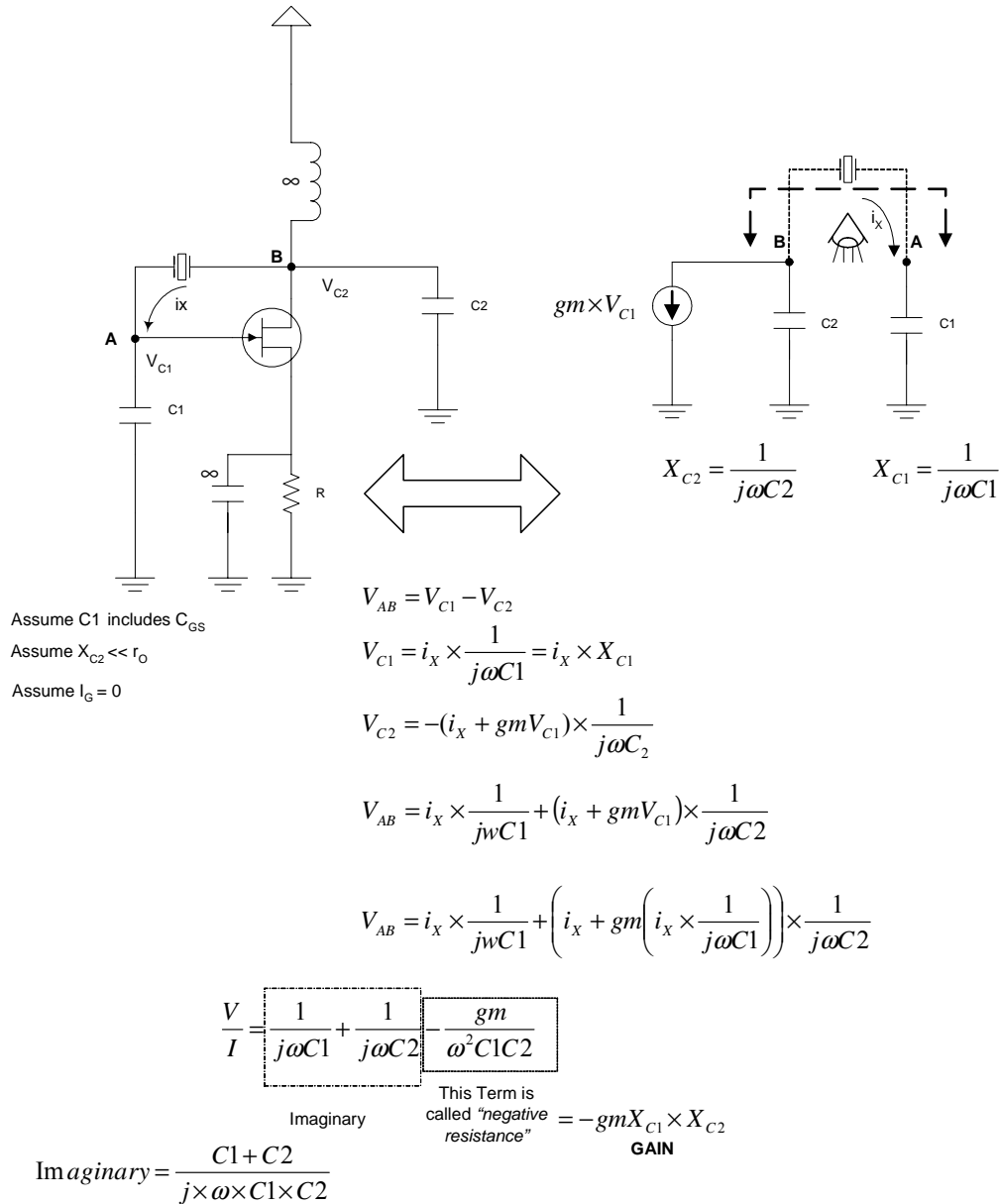

Assume C1 includes C_{GS}

Assume $X_{C2} \ll r_O$

Assume $I_G = 0$

$$X_{C2} = \frac{1}{j\omega C2} \qquad X_{C1} = \frac{1}{j\omega C1}$$

$$V_{AB} = V_{C1} - V_{C2}$$

$$V_{C1} = i_X \times \frac{1}{j\omega C1} = i_X \times X_{C1}$$

$$V_{C2} = -(i_X + gmV_{C1}) \times \frac{1}{j\omega C_2}$$

$$V_{AB} = i_X \times \frac{1}{jwC1} + (i_X + gmV_{C1}) \times \frac{1}{j\omega C2}$$

$$V_{AB} = i_X \times \frac{1}{jwC1} + \left(i_X + gm\left(i_X \times \frac{1}{j\omega C1} \right) \right) \times \frac{1}{j\omega C2}$$

$$\frac{V}{I} = \boxed{\frac{1}{j\omega C1} + \frac{1}{j\omega C2}} \boxed{- \frac{gm}{\omega^2 C1C2}}$$

Imaginary

This Term is called *"negative resistance"* $= -gm X_{C1} \times X_{C2}$

GAIN

$$\mathrm{Im}\,aginary = \frac{C1 + C2}{j \times \omega \times C1 \times C2}$$

Fig. 4: Negative Resistance Derivation

The familiar term:

$$-R = -gm \cdot X_{C1} \cdot X_{C2},$$

describes the negative resistance of the active network as a function of the gm, or transconductance, of the active device along with the reactance value of the two Pierce capacitors, C1 and C2. One can see that in order to raise the negative resistance from the active network you have to raise the gm or lower the capacitance of the two Pierce

capacitors. The design limit being that in the case of C1 and C2 the crystal manufacturer will not generally specify the crystal load capacitance, CL, below a value of 8 pF:

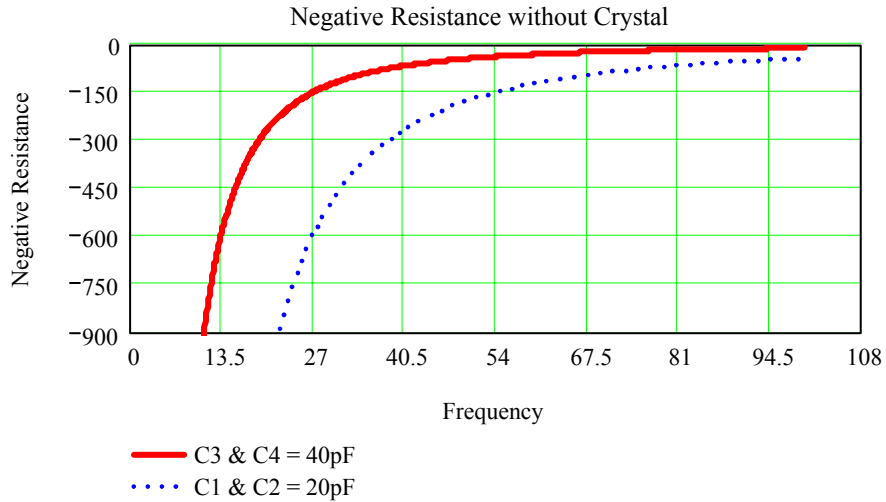$$CL = \left[\frac{C1 \times C2}{C1 + C2} \right]$$

Negative Resistance without Crystal

Fig. 5: Negative Resistance Vs. C1 and C2

This sets the lower limit of C1 and C2 at 16 pF each since it is their series combination including strays that comprises the load seen by the crystal, CL. The design limit for the active device in the case of gm is its size.

Fig. 5 illustrates the change in negative R with respect to C1 and C2. At the frequency of 27 MHz the negative resistance is 600 Ω for C1 and C2 equal to 20 pF each. One can see that the negative resistance with C3 and C4 equal to 40 pF each has now dropped at 27 MHz to 150 Ω.

This is the point in the analysis where most people will stop and require the semiconductor manufacturer to supply an active network with a specific negative resistance based on an arbitrary design rule of thumb, never having specified the crystal!

The addition of the crystal to the active network will drastically change the value of negative resistance that the active network can provide. The crystal as an equivalent network and the active network must now be analyzed as a whole. Fig. 6 is a negative-resistance model of an oscillator with the crystal connected as the motional branch.
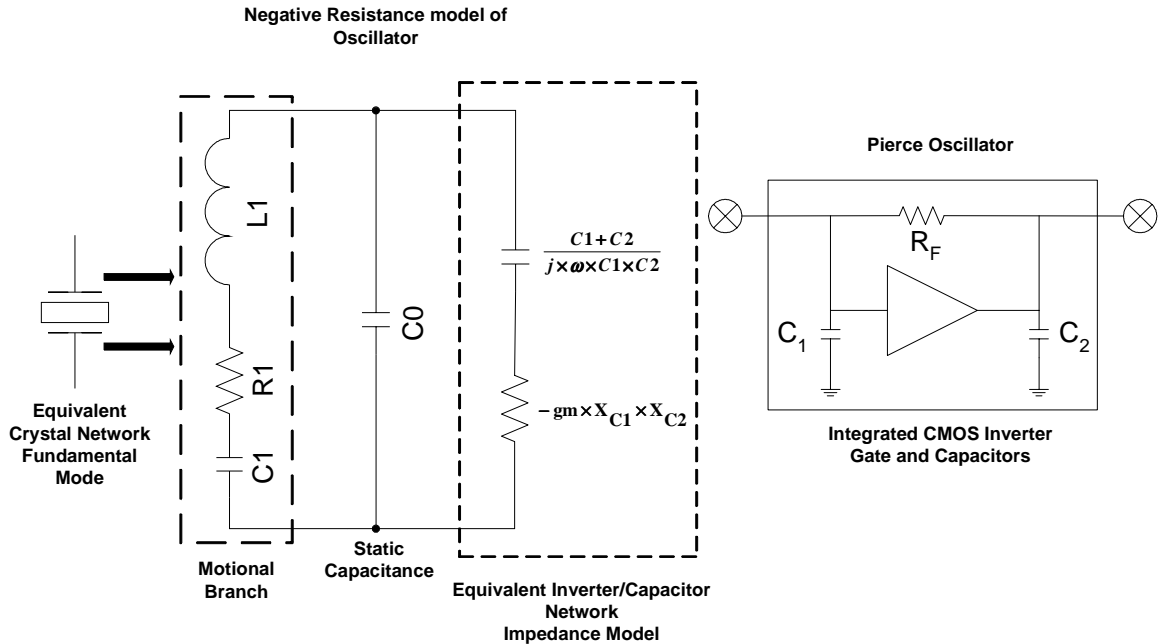
Fig. 6 Negative-Resistance Oscillator Model

Not only does the crystal supply a motional branch necessary in forming an oscillator circuit but along with it comes an additional capacitance C0 (refer to Fig. 3 for the crystal model and description). The shunt capacitance dramatically alters the behavior of the active network and severely limits the amount of negative resistance that can be supplied.
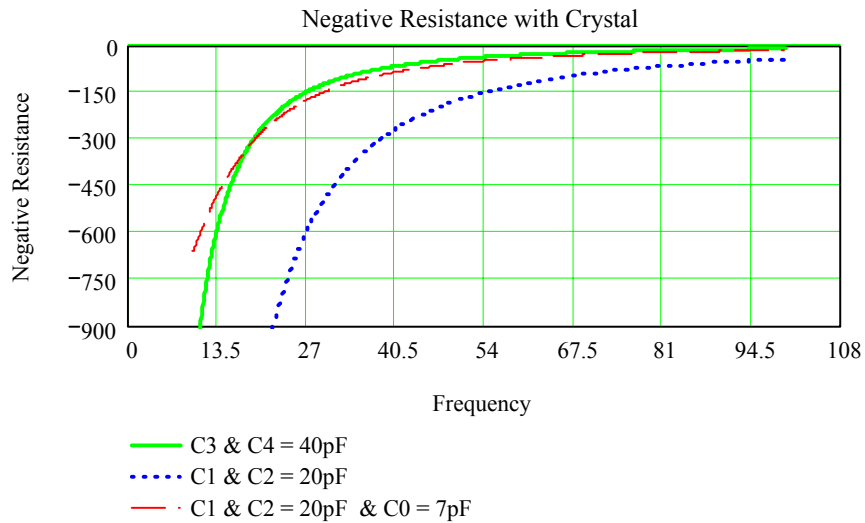

Fig. 7: Negative Resistance With & Without C0

Fig. 7 shows the effect on negative resistance when a crystal with a C0 of 7 pF is added to a circuit with C1 and C2 both of 20 pF. The negative resistance at 27 MHz drops from 600 Ω to about 150 Ω, equaling the value when C3 and C4 were both 40 pF with no crystal added. C0 is an intrinsic property of the crystal and cannot be ignored. This is why the crystal vendor, customer, and the semiconductor manufacturer must communicate and agree on design goals and measurement methodology.

Due to the contribution of C0 an active network that delivered 600 Ω at 27 MHz without the crystal will not achieve a negative resistance of 600 Ω when combined with a crystal with a 60-Ω resistance and a C0 of 7pF. This circuit will not satisfy a negative resistance design rule of thumb of ten times the motional resistance. Fig. 8 demonstrates the effect on negative resistance when the same active network is attached to two different crystals with varying C0s. C0 is proportional to the physical size of the crystal, electrode size. VCXOs generally require a larger C1 that translates into a larger electrode. A larger metal can crystal will have a larger C0 than a smaller SMD type crystal. That is why an engineer should not use a negative resistance rule of thumb in oscillator design.
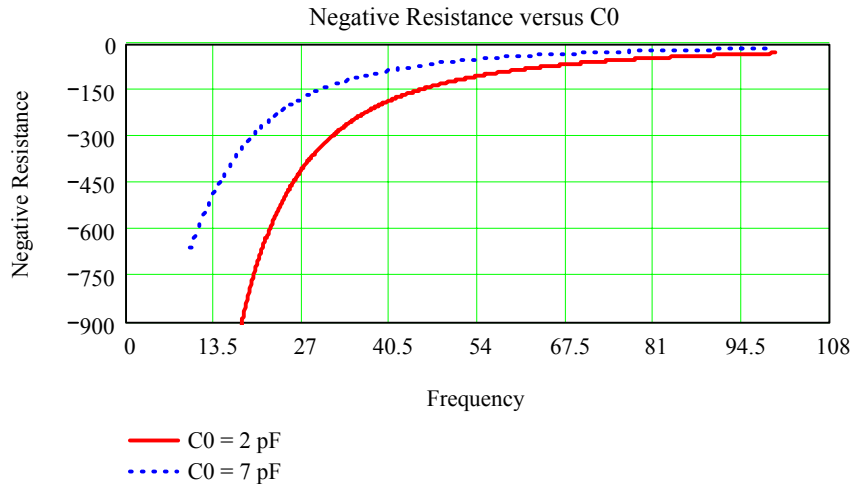

Fig. 8: Negative Resistance Versus Crystal C0

We have now shown that the crystal and the active element should both be analyzed as a whole for any given oscillator application. Choice of negative R or the active element gain does not have to be left up to generic rules of thumb. There is a mathematical way to choose the optimal negative resistance and gm, transconductance for any given active network and crystal pair. Eric Vittoz presented this in a paper presented in the IEEE Journal of Solid State circuits. [1]

The first equation relates the maximum negative R obtainable with a crystal and Pierce oscillator circuit where C0 and C1 and C2 are known. This is the standard case for any given oscillator configuration. Equation 1 is an expression for the maximum obtainable negative resistance. This maximum negative R occurs at an optimum gm, transconductance, value and is given in equation 2.

$$R_{N(MAX)} = \frac{-1}{2\omega \cdot C0\left(1 + C0\dfrac{C1+C2}{C1C2}\right)}$$

Equation 1

$$gm_{OPT} = \omega\left(C1+C2+\frac{C1C2}{C0}\right)$$

Equation 2

The following diagram (Fig. 9) taken from Vittoz's paper illustrates the effect of varying gm. If the transconductance of the active device is increased beyond the optimal value then there is a decrease in negative resistance and a region is approached where no oscillation can occur. In applying an arbitrary rule of thumb the end user can now reach a point where instead of safeguarding and creating a gain margin in their design they have now created the same effect of having not enough negative resistance. Their oscillator circuit will not start.
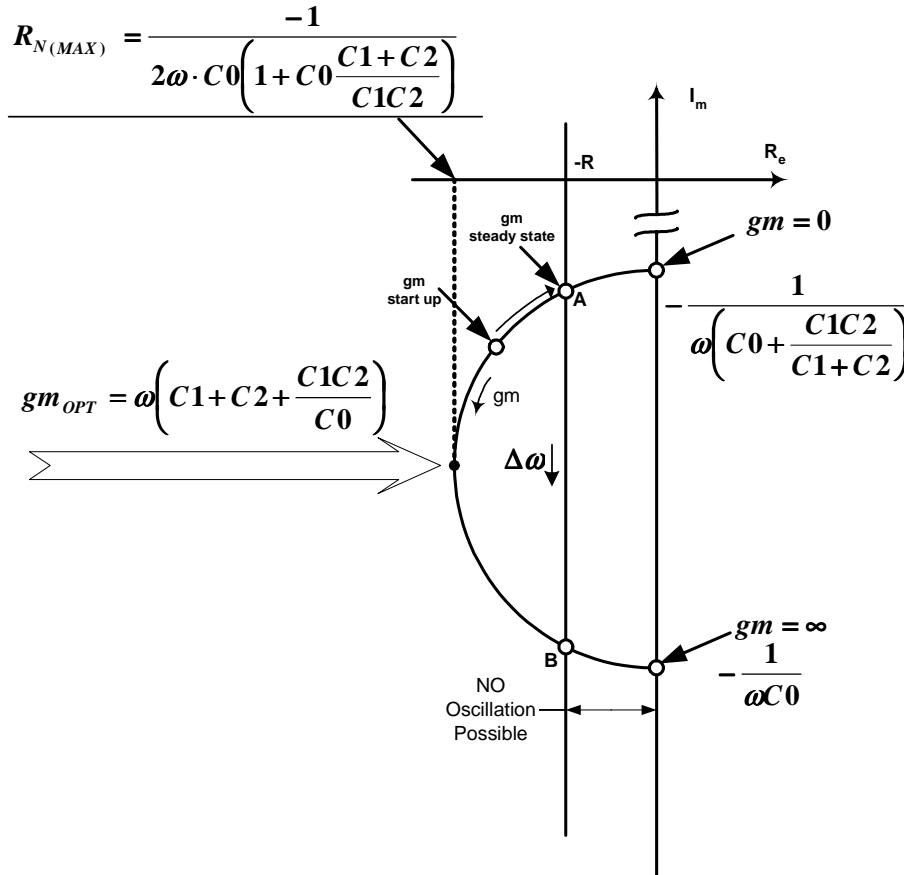

$$R_{N(MAX)} = \frac{-1}{2\omega \cdot C0\left(1 + C0\dfrac{C1+C2}{C1C2}\right)}$$

$$gm_{OPT} = \omega\left(C1 + C2 + \frac{C1C2}{C0}\right)$$

$$-\frac{1}{\omega\left(C0 + \dfrac{C1C2}{C1+C2}\right)}$$

$$-\frac{1}{\omega C0}$$

$gm = 0$

$gm = \infty$

Fig. 9: Complex Plane Representation Of Lossless Three-Point Oscillator (From Vittoz)

As gm is increased past the optimal point the obtainable negative resistance actually decreases and enters a region where the oscillator will no longer start. If the active device gain was set by an arbitrary rule of thumb to satisfy a specified negative-resistance value and then later combined with a crystal that had a certain C0 the end result can be that the oscillator will never start. This can easily happen as devices are designed and sold to cover a broad range of markets and applications. Circuits can no longer be custom-tailored to specific applications, as this is not an economically viable business strategy. A set top box (STB) application may require a larger crystal based on cost alone whereas a handheld application demands the use of a small SMD crystal. The active element must now be able to properly function with crystals of varying parameters.

In conclusion we now have the ability to take any given crystal oscillator requirement and design and compute the optimal negative resistance based on the proper application and manufacturing process constraints. This ensures a robust oscillator design. Cypress offers a high degree of design flexibility with the use of programmable die and strong product support. Our programmable die allows us to choose the optimal gm and the correct negative resistance for any given configuration.

References

[1] E Vittoz *High-Performance Crystal Oscillator Circuits: Theory and Application* IEEE Journal of Solid State Circuits, Vol 23, No 3, June 1988 pp 774 - 783.
[2] Benjamin Parzen with Arthur Ballato, *Design of Crystal and Other Harmonic Oscillators* 1983, a Wiley-Interscience publication: division of John Wiley & Sons, Inc.

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