Double Edge-Triggered D-Flip-Flops for High-Speed CMOS Circuits

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Abstract—**A double edge-triggered D-flip-flop (DETDFF) responds to both edges of the clock pulse. As compared with positive or negative edge-triggered flip-flops, a DETDFF has advantages in terms of power dissipation and speed. Two CMOS implementations of DETDFF are presented. These designs are suitable for high-speed CMOS circuits.**

I. Introduction

ALMOST all contemporary digital VLSI systems and other digital systems rely on clock pulses to control the movement of data. Clocking can easily be discussed in connection to a finite-state machine, as shown in Fig. 1. Input signals together with present state signals are inputs to a combinational logic block whose outputs are outputs and next-state signals of the machine. Several different types of flip-flops or latches may be used for the storage element. If, for example, a positive edge-triggered D-flip-flop (ETDFF) is used as the storage element, at the positive clock edge, the next state becomes the present state and a new state is generated. The circuit will be safe, if the flip-flop is always nontransparent: that is, a state signal cannot pass the logic block more than once during one clock cycle. Designing circuits with ETDFF's is rather simple and straightforward [1], [2]. In a study [1], however, it was concluded that ETDFF's could not be used for high-speed designs. This conclusion is based on an assumption that clock skew between two communicative modules may be positive for the current clock cycle and negative for the next clock cycle. Sources of clock skew in a VLSI chip may be unequal clock path delay, process variation, and temperature fluctuations. It is not probable that these parameters change during one clock period in a digital VLSI chip. However, propagation delay in flip-flops is usually longer than latches as their structures are more complicated. But if the combinational logic circuit has longer delay compared with the flip-flops, minor extra delay in flip-flops may be insignificant.

The timing behavior of a positive ETDFF is shown in Fig. 2. The input data D must be valid during the interval given by the setup U and hold H times of the device. The output data Q are available and stable D_{CQ} after the active clock edge. It is also possible to design a device that is triggered on the negative clock edge instead of on the positive edge.

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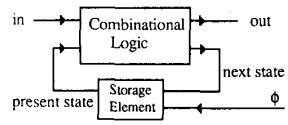

Fig. 1. State machine diagram.

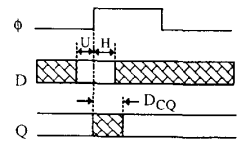

Fig. 2. Timing parameters of a positive ETDFF.

It may be noted from Fig. 2 that, during each clock period, the negative edge of the clock signal accomplishes nothing, although it may change the state of some devices inside the flip-flop. This redundancy may have important consequences for future VLSI systems. In CMOS, which is the main technology of VLSI, power is dissipated only when a transition occurs. When feature sizes are scaled down, delay in the interconnection lines increases quadratically with the line length. This will have determining effects on the time performance of synchronous systems as it increases the clock skew drastically. In order to reduce the delay in lines and make it linear with the line length, repeaters (inverters) should be inserted along the lines [3]. This, in fact, is a trade-off between power and speed. These repeaters consume power during both transitions. If flip-flops could be triggered on both edges of the clock pulses instead of on only one edge, it would be possible to use a clock at half frequency for the same data rate, thus reducing the power dissipation of the clock distribution network. Two circuits have previously been reported for double ETDFF's (DETDFF's) [4], [5]. These circuits are, however, slow and have rather high transistor counts. This paper proposes two new circuits for DETDFF that are fast and simple. These circuits can be used in high-speed CMOS designs.

II. DETDFF Circuit Realization

A DETDFF can be constructed by using two complementary latches in parallel. One latch must react on the positive edge of the clock pulse and the other must react on the negative edge. Then a merging circuit may be used to merge the two outputs from the two latches into a single output. The circuit for a dynamic positive ETDFF

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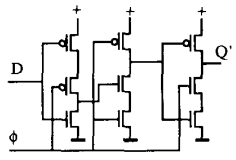

Fig. 3. Circuit diagram of a dynamic D-flip-flop.

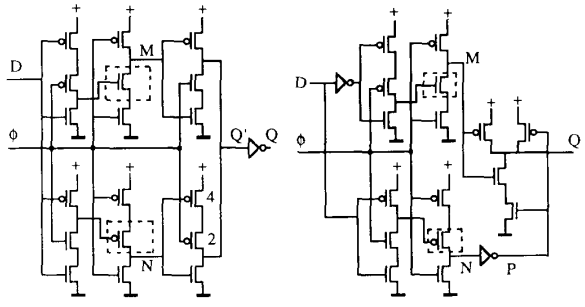

Fig. 4. Two circuits for DETDFF. Numbers in (a) are relative width sizes of these transistors to the minimum-size transistor.

is shown in Fig. 3. A negative ETDFF can be constructed by complementing this circuit [6].

During the positive part of the clock pulse, depending on the value of input D at the setup time prior to the positive edge of the clock pulse, the output node will be either pulled up or down. During the negative part of the clock pulse the output is latched and the output node will be a high-impedance node. The circuit for a negative ETDFF has a complementary behavior, i.e., its output is in a high-impedance mode during the positive part of the clock pulse and has a path to ground or to the power supply during the negative part of the clock pulse. Thus, if the output of a positive ETDFF is directly connected to the output of a negative ETDFF, they not only do not fight against each other, rather, they complement each other such that when the output of one of the circuits is a high-impedance node it lets the other circuit decide the output value and vice versa. In Fig. 4(a) the complete circuit of a DETDFF constructed from positive and negative ETDFF's is depicted. The merging circuit for this circuit is only an interconnection line that connects the outputs of the two circuits.

Clock loading for the circuit in Fig. 4(a) may be considered excessive in some situations. It is possible to construct another circuit for a double ETDFF that has less clock loading. Consider nodes M and N in Fig. 4(a). When the clock is low, node M is precharged to high. When the clock is high this node evaluates the latched input data. Node N, compared with node M, has a complementary behavior. This property is used in Fig. 4(b), which shows another circuit for the double ETDFF. The merging circuit for this circuit is a NAND circuit. Referring to Fig. 4(b), notice that, when the clock is low, node M is precharged to high and lets the node P value decide the output of the NAND gate. When the clock is high, node N is precharged to low and P becomes high. Thus, node M decides the NAND output value. In this way, the two parallel branches alternatively determine the output and a DETDFF is thus obtained. Two inverters, inserted in this circuit, are used for the sake of polarity compatibility.

III. DETDFF Timing

It is straightforward to show that the maximum clock period of the state machine in Fig. 1 is

$$P \geqslant D_{CQ} + U + D_L \tag{1}$$

where D_{CO} and D_L are the delays in the flip-flop and combinational circuits, respectively, and U is the setup time of the flip-flop. Thus the delay contribution of the flip-flop to the clock period is $D_{CQ} + U$. This parameter may be called the delay figure of the flip-flop. In order to measure delay figures for the two DETDFF's, consider that, if the Q output from the DETDFF is fed to an odd number of inverter chains and back to the flip-flop input, a ring oscillator is formed (see Fig. 5(a)). Then, to measure the time figure of the flip-flops, the frequency of the clock pulse is gradually increased up to a point where the oscillator fails to operate. The timing diagram for the oscillator at this frequency is as shown in Fig. 5(b).

In this figure, D_L is the inverter chain delay. Then, to calculate the maximum operating frequency of the flip-flops, $D_{L1} + D_{L2}$ must be subtracted from the clock period. We implemented the two DETDFF's in a 2-μm CMOS process and simulated the extracted circuit with SPICE. When all transistors have a practical minimum size, that is, when their gate width is 6 μm and their gate length is 2 μm, the maximum clock frequency of the flip-flop in Fig. 4(a) and (b) is 320 and 350 MHz, respectively. A minor change in the size of the output stage of the negative ETDFF in Fig. 4(a) increases the maximum operating frequency of this flip-flop to 400 MHz. Numbers in Fig. 4(a) show the relative width sizes of these transistors to the minimum-size transistor. Fig. 5(c) depicts the SPICE simulation results for the flip-flop in Fig. 4(a). In this simulation, only one inverter is used in the feedback circuit. Table I summarizes the comparison between the proposed flip-flops with the circuit in [5].

One disadvantage of the DETDFF is that its output cannot be applied to precharged dynamic circuits, because it is not stable during either high or low parts of the clock pulse. However, logic circuits can be included within the DETDFF circuit. The n-channel and p-channel transistors, marked by dotted-line squares in Fig. 4, may be replaced by n-channel and p-channel transistor networks. For example, the n-channel and p-channel transistors may be replaced by the circuits shown in Fig. 6(a), (b), or a combination of them to provide a set, reset, or set/reset for the flip-flops.

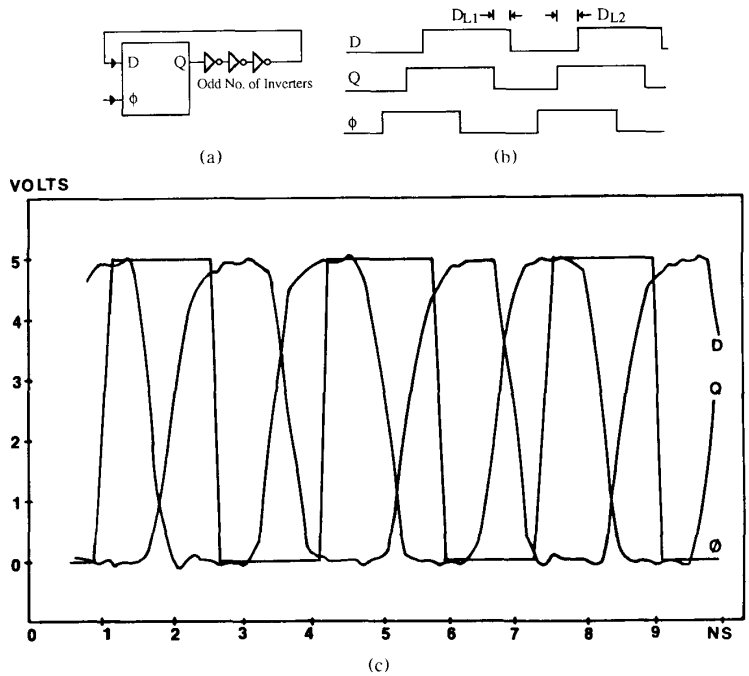

Fig. 5. (a) Ring oscillator. (b) Timing diagram. (c) SPICE simulation results.

TABLE I
IMPLEMENTATIONS COMPARISON

	No. of Transistors	Equ. Load of Clock Pulse	Max. Operating Clock Frequency
Circuit in [5]	28*	$6C_g$	50 MHz
Fig. 4(a)	20	$8C_g$	320–400 MHz
Fig. 4(b)	20	$6C_g$	350 MHz

*Including two transistors for data inversion

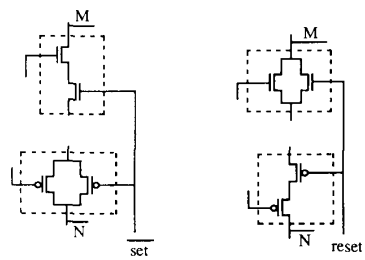

Fig. 6. Set and reset circuits for the flip-flops.

IV. CONCLUSIONS

Two circuits are proposed for double edge-triggered flip-flops. Delay figures for these circuits are measured by simulation. It is shown that these circuits are faster and have fewer transistor counts than previously reported circuits. It is shown that these flip-flops can be used at 320–400-MHz clock frequency in a 2-μm technology.

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